Abstract

A network processor or other type of processor includes classification circuitry and memory circuitry coupled to the classification circuitry. The memory circuitry is configured to store at least a portion of at least a given one of a number of packets to be processed by the classification circuitry. The classification circuitry implements a non-sequential packet classification process for at least a subset of the packets including the given packet. For example, in an embodiment in which the given packet is generated in accordance with multiple embedded protocols, the non-sequential packet classification process allows the processor to return from a given point within the packet, at which a final one of the protocols is identified, to a beginning of the packet, through the use of a "skip to beginning" instruction. The skip to beginning instruction may be configured to allow the processor to skip back to a particular bit, e.g., a first bit, of the given packet at a time during the classification process after which the particular bit has been processed, such that multiple passes of the classification process can be performed on the given packet. The processor may be configured as a network processor integrated circuit to provide an interface between a network from which the packet is received and a switch fabric in a router or switch.